Quartus II と ModelSim の使い方 (概要)

- 1. If Quartus II 13.1.0.162 was not installed in your PC, download from CIS Storage Server and install it (ModelSim will be installed together automatically)
- 2. Before running Quartus II 13.1, create a working directory (フォルダー), Documents\cod_cpu for example (do not use 全角 characters)
- 3. Circuit design and simulation
 - (a) Start Quartus II 13.1
 - i. Create a project in the created working directory
 - ii. Use schematic capture to create circuit
 - iii. Circuit analysis & synthesis; if there are errors, correct circuit
 - iv. Create Verilog HDL file from the circuit
 - v. Create Verilog HDL file (test bench) for simulation
 - (b) Start ModelSim-Quartus 10.1d
 - i. Change directory to the working directory
 - ii. Compile Verilog HDL files
 - iii. Simulate by using the test bench
 - iv. Check waveform; if there are errors, correct circuit; go to (a) iii
 - (c) In Quartus II, create circuit symbol for later use

Create a Working Directory

First of all, create a folder, for example

 $C: \ Users \ your_account \ Documents \ cod_cpu$

Your all designs must be done in this folder

Start Quartus II 13.1





Quartus II と ModelSim の使い方-3/31

New Project — mux2x1

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Working Directory and Project Name

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New Block Diagram/Schematic File





Quartus II と ModelSim の使い方 - 6 / 31



Quartus II と ModelSim の使い方 – 7 / 31

Input Gates and Pins



Assign Pin Names



法政大学情報科学部

Quartus II と ModelSim の使い方 – 9/31



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Quartus II と ModelSim の使い方 – 10 / 31

Start Analysis & Synthesis



Create Verilog HDL Design File





New Verilog HDL Testbench File



Code of Verilog HDL Testbench File

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Start ModelSim-Quartus 10.1d

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Add Signals to Wave Window

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<pre># Top level modules: # mux2x1</pre>			
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Quartus II と ModelSim の使い方 – 20 / 31

Run Simulation

Create Block Symbol for Future Use

New Project — mux2x8

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Project Navigator		^	
Compilation Hierarchy	Directory, Name, Top-Level Entity [page 1 of 5]		
	What is the working directory for this project?		
	C:\Users\yamin\Documents\cod_cpu		
	What is the name of this project?		
	mux2x8		
	What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.		
	mux2x8		
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Input Components

Quartus II と ModelSim の使い方 – 24 / 31

Use Wire Names to Connect Pins

Start Analysis & Synthesis

Add Project mux2x1.bdf

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Start Analysis & Synthesis

法政大学情報科学部

Code of Testbench File mux2x8_tb.v

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Entity Cyclone IV GX: AUTO Mux2x8	<pre>1 'timescale lns/lps // unit = 1 ns; accuracy = 1 ps 2 module mux2x8_tb; // test bench, no input / output pins 3 reg [7:0] A0,A1; // reg type for inputs of mux2x1 (8 bits) 4 reg S; // reg type for outputs of mux2x1 (1 bit) 5 wire [7:0] Y; // wire type for outputs of mux2x1 (8 bits) 6 mux2x8 i1 (.A0(A0), .A1(A1), .S(S), .Y(Y)); // invoke mux2x8 7 initial begin // input signal patterns 8</pre>		^
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Simulation with ModelSim

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#		
<pre># Top level modules: # mux2x8</pre>		
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#		
# Top level modules:		
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# vsim -gui work.mux2x8_tb		
<pre># Loading work.mux2x8_tb</pre>		
<pre># Loading Work.mux2x8 # Loading Work.mux2x1</pre>		
VSIM 23> add wave /*		
VSIM 24> run		
# Break in Module mux2x8_tb at C:/Us	sers/yamin/Documents/cod_cpu/mux2x8_tb.v line 12	
VSIM 25>		-

Create Block Symbol for Future Use

