Quartus II と ModelSim の使い方 (概要)

1. If Quartus II 13.1.0.162 was not installed in your PC, download from CIS Storage Server and install it (ModelSim will be installed together automatically)
2. Before running Quartus II 13.1, create a working directory (フォルダー), Documents\cod_cpu for example (do not use 全角 characters)
3. Circuit design and simulation

   (a) Start Quartus II 13.1

      i. Create a project in the created working directory
      ii. Use schematic capture to create circuit
      iii. Circuit analysis & synthesis; if there are errors, correct circuit
      iv. Create Verilog HDL file from the circuit
      v. Create Verilog HDL file (test bench) for simulation

   (b) Start ModelSim-Quartus 10.1d

      i. Change directory to the working directory
      ii. Compile Verilog HDL files
      iii. Simulate by using the test bench
      iv. Check waveform; if there are errors, correct circuit; go to (a) iii

   (c) In Quartus II, create circuit symbol for later use

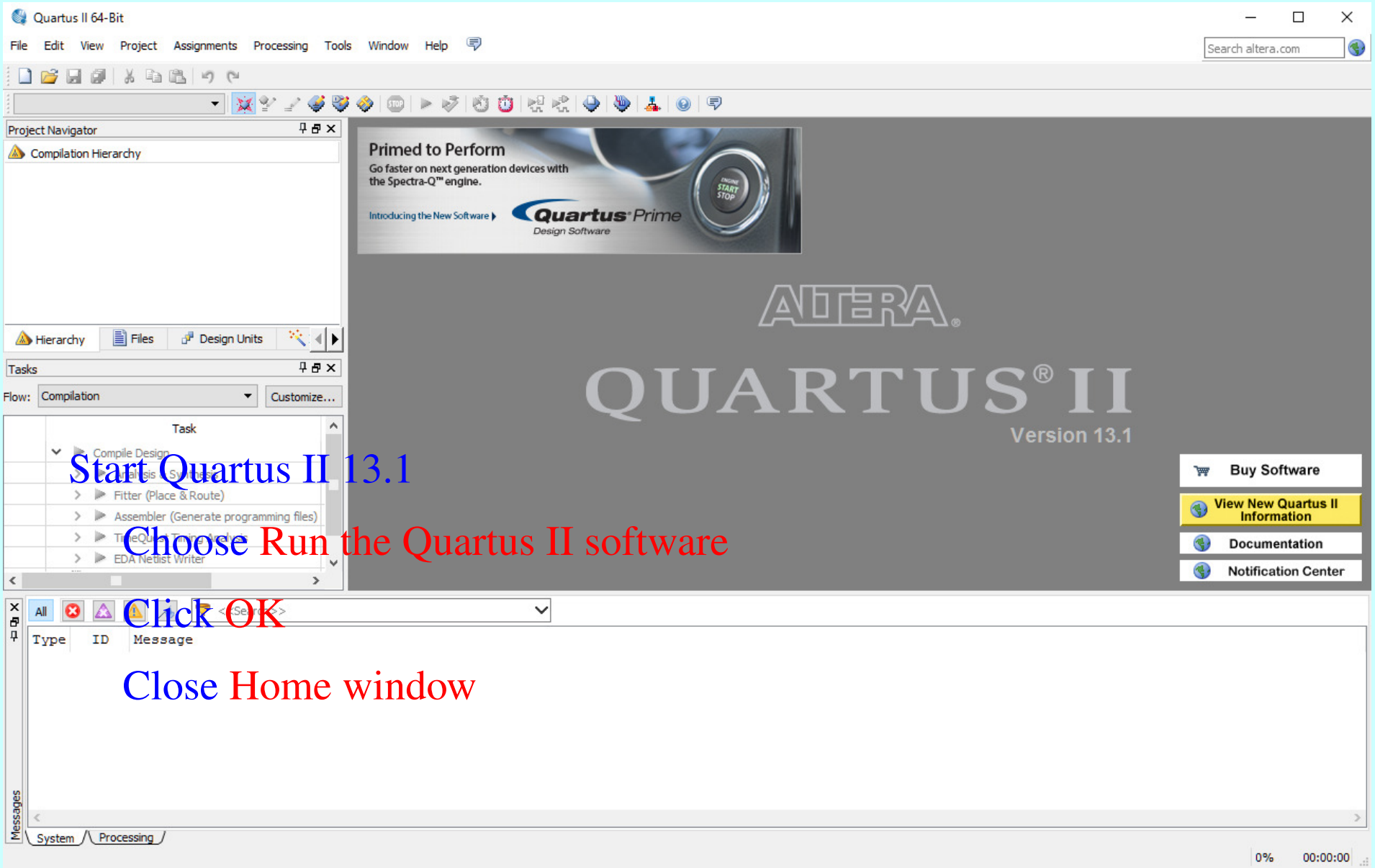
Create a Working Directory

First of all, create a folder, for example

C:\Users\your_account\Documents\cod_cpu

Your all designs must be done in this folder

Start Quartus II 13.1



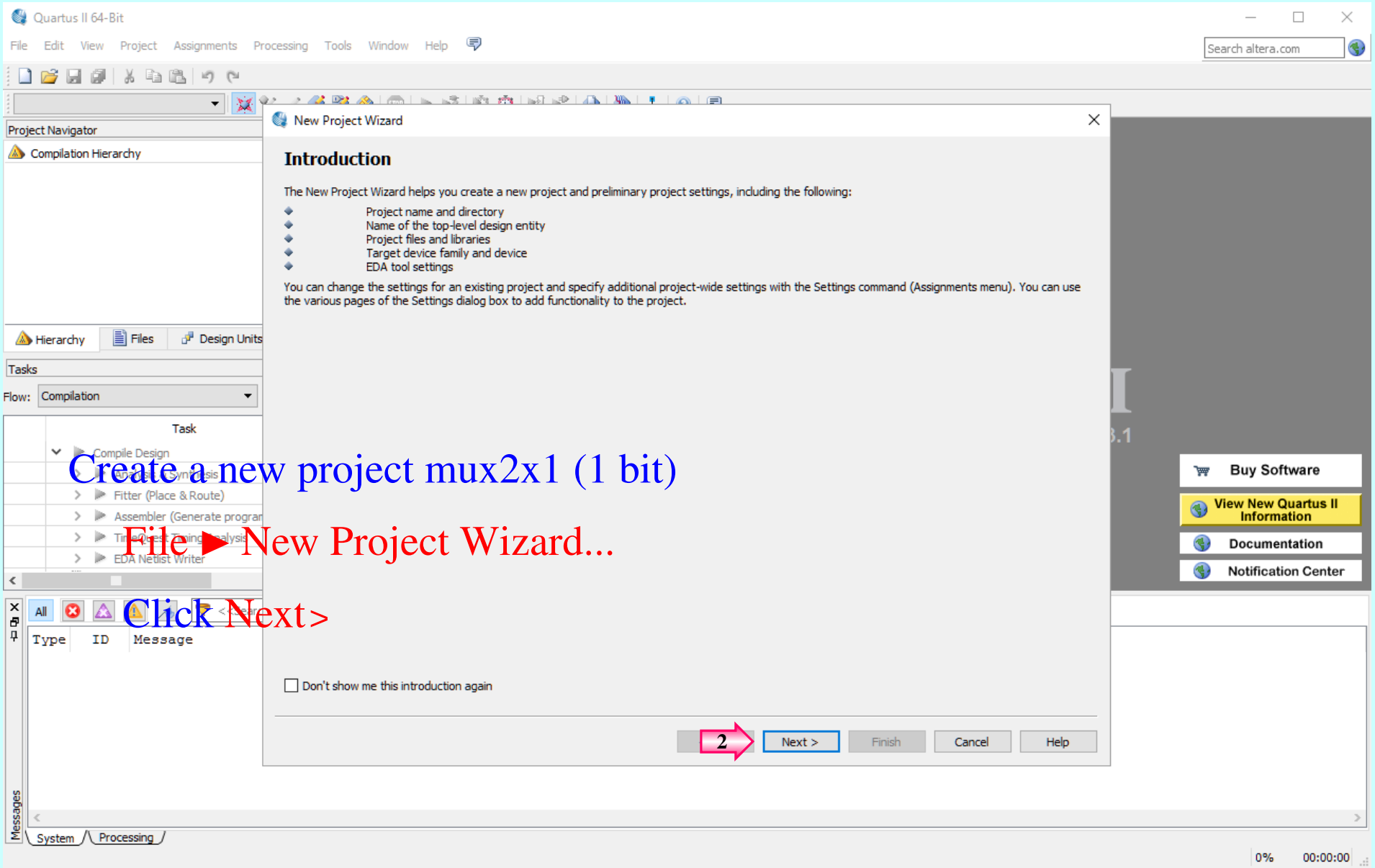
Start Quartus II 13.1

Choose Run the Quartus II software

Click OK

Close Home window

New Project — mux2x1

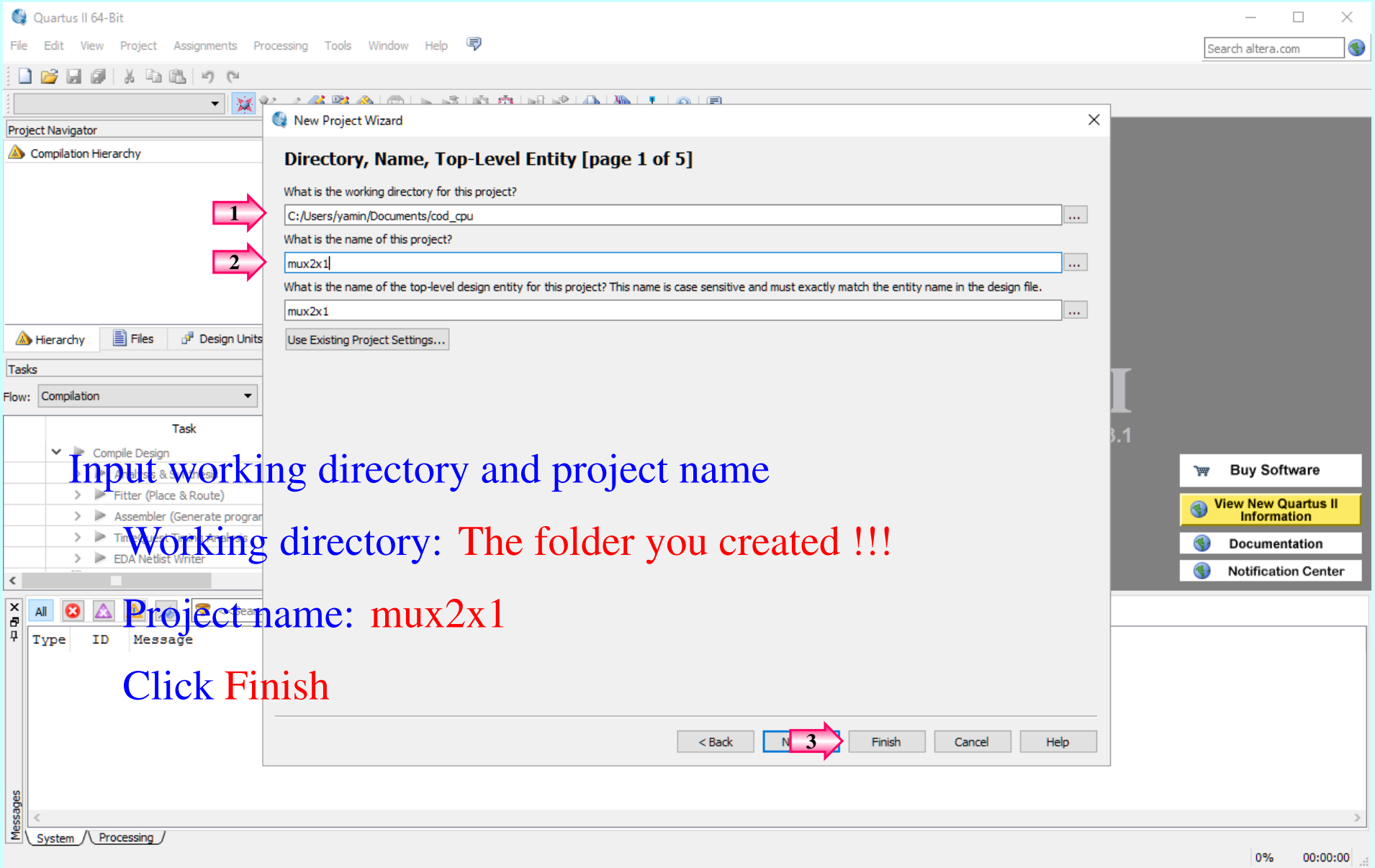


Create a new project mux2x1 (1 bit)

File ► New Project Wizard...

Click Next>

Working Directory and Project Name



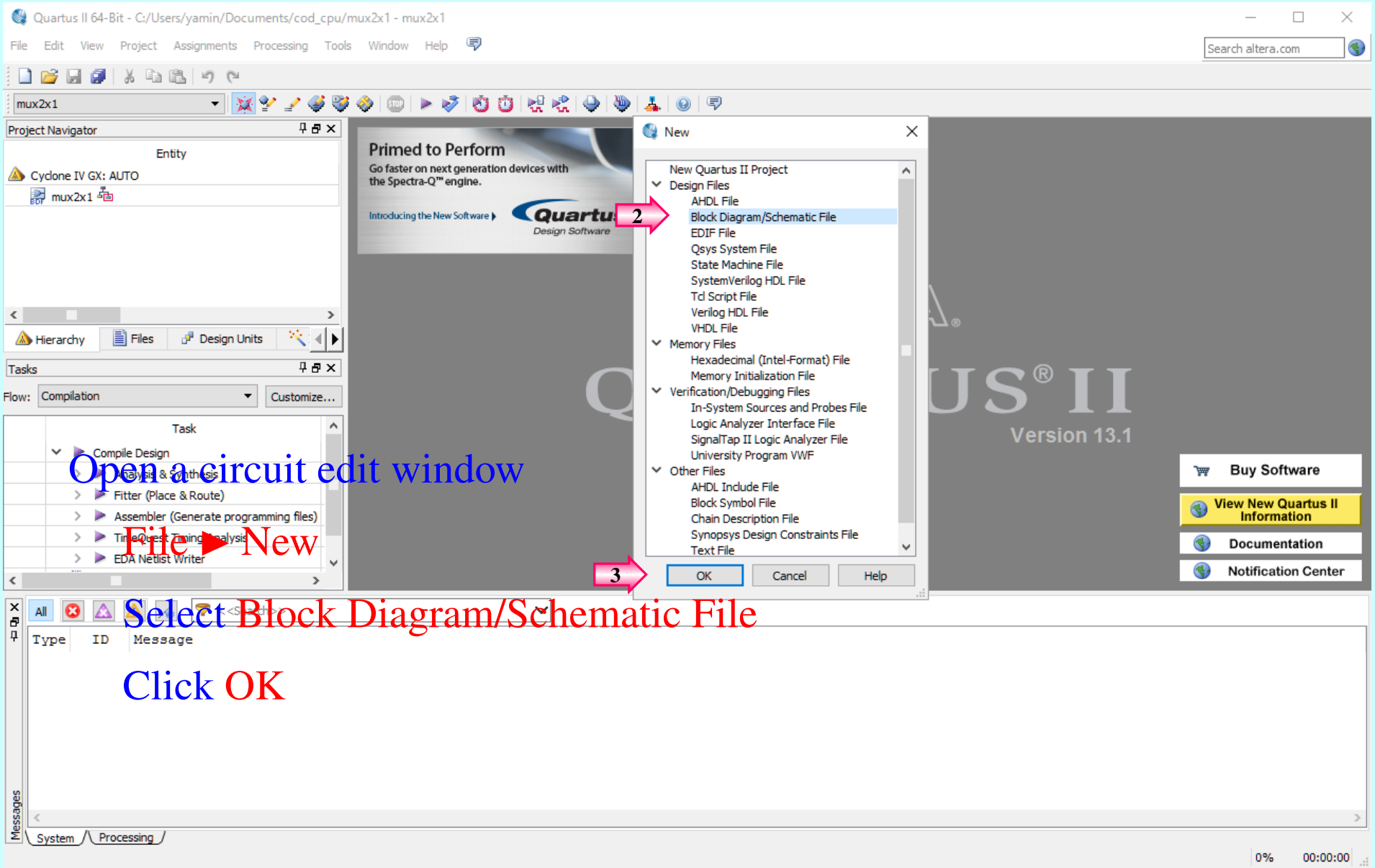
Input working directory and project name

Working directory: The folder you created !!!

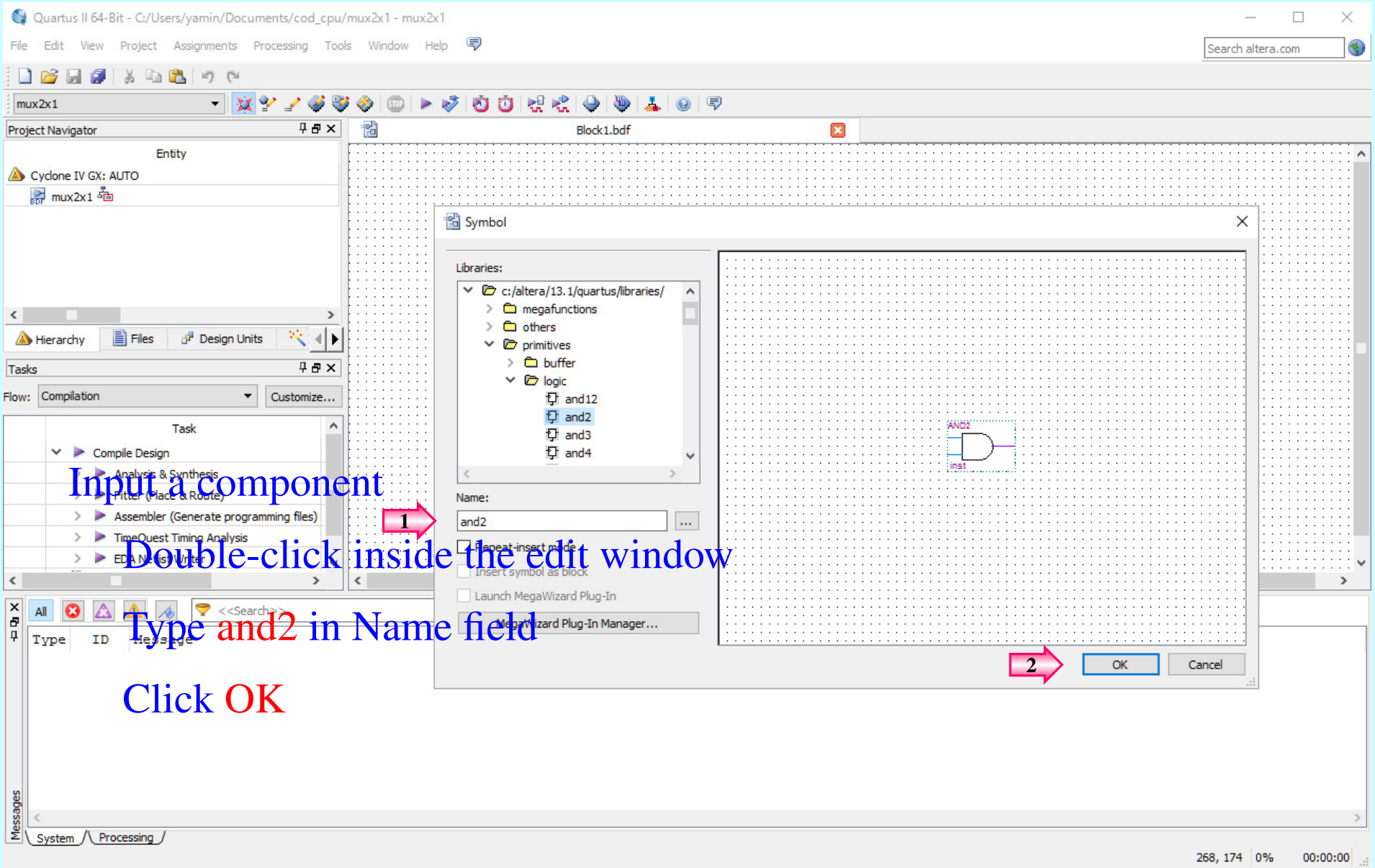
Project name: mux2x1

Click Finish

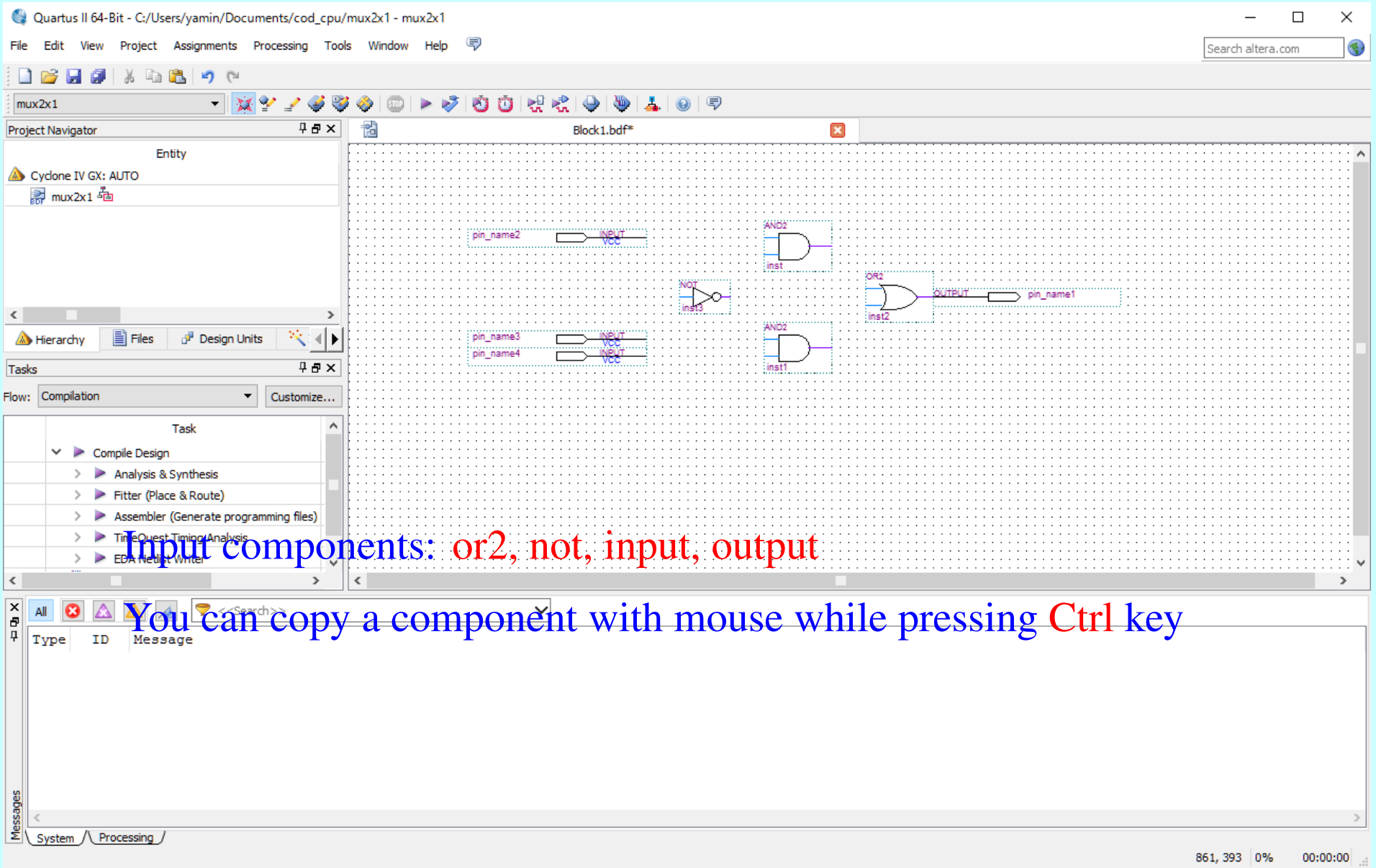
New Block Diagram/Schematic File



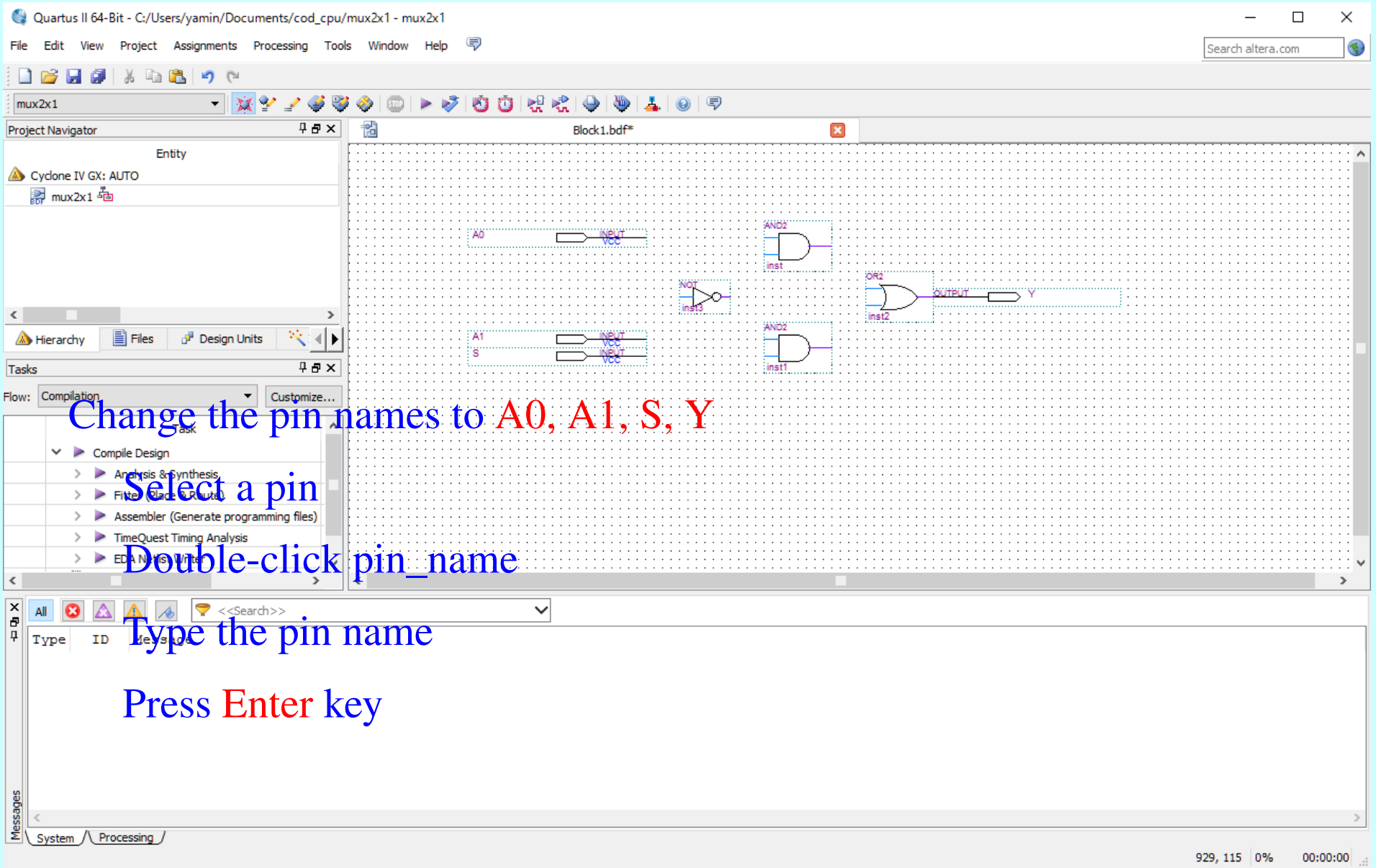
Input Gates


Input a component
Double-click inside the edit window
Type and2 in Name field
Click OK
1
2
Symbol
Libraries:
c:/altera/13.1/quartus/libraries/
megafunctions
others
primitives
buffer
logic
and12
and2
and3
and4
Name:
and2
Repeat-insert mode
Insert symbol as block
Launch MegaWizard Plug-In
MegaWizard Plug-In Manager...
OK
Cancel
Block1.bdf
Project Navigator
Entity
Cyclone IV GX: AUTO
mux2x1
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Assembler (Generate programming files)
TimeQuest Timing Analysis
Type
ID
Message
System
Processing
268, 174
0%
00:00:00

Input Gates and Pins



Assign Pin Names



Change the pin names to A0, A1, S, Y

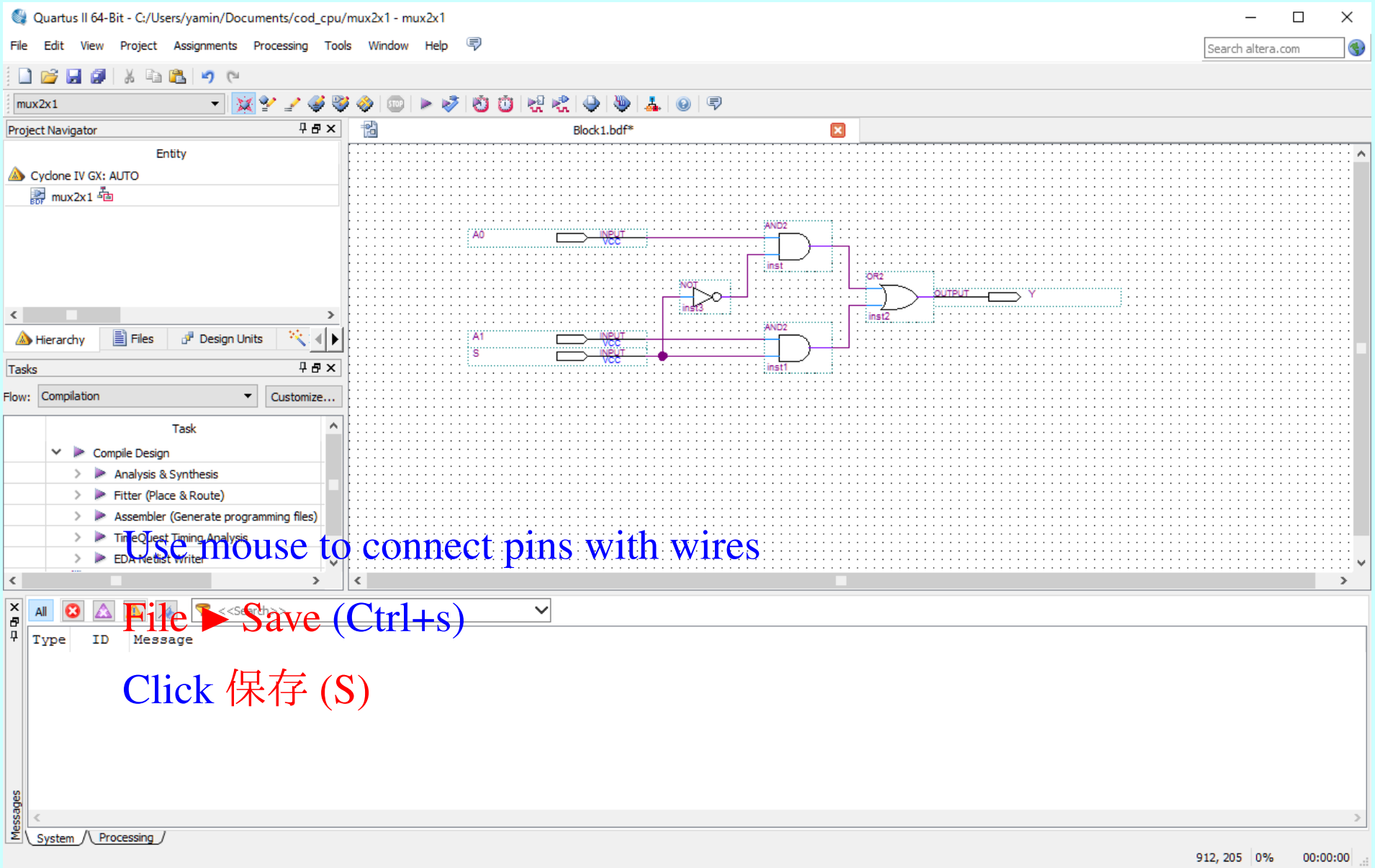
Select a pin

Double-click pin_name

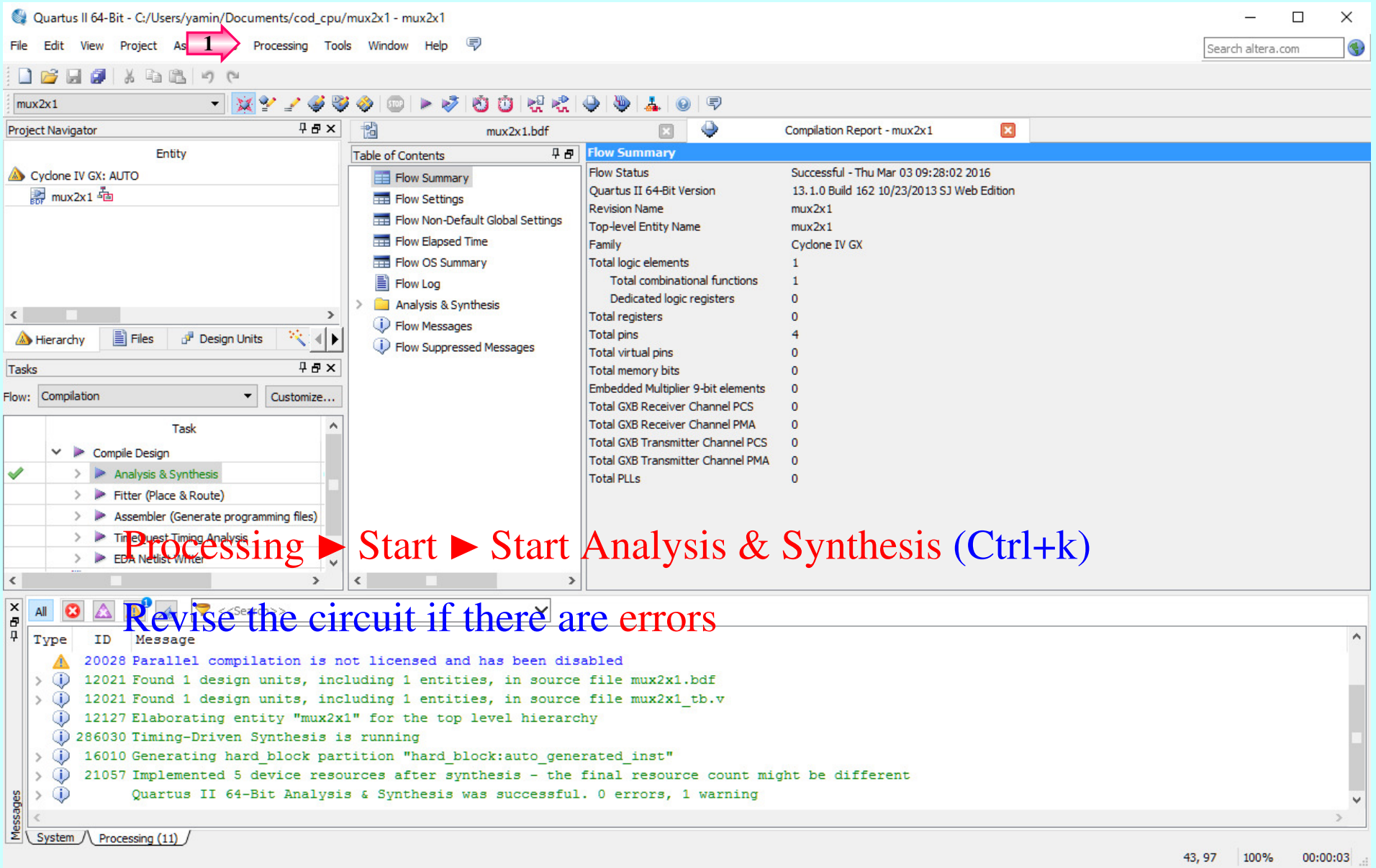
Type the pin name

Press Enter key

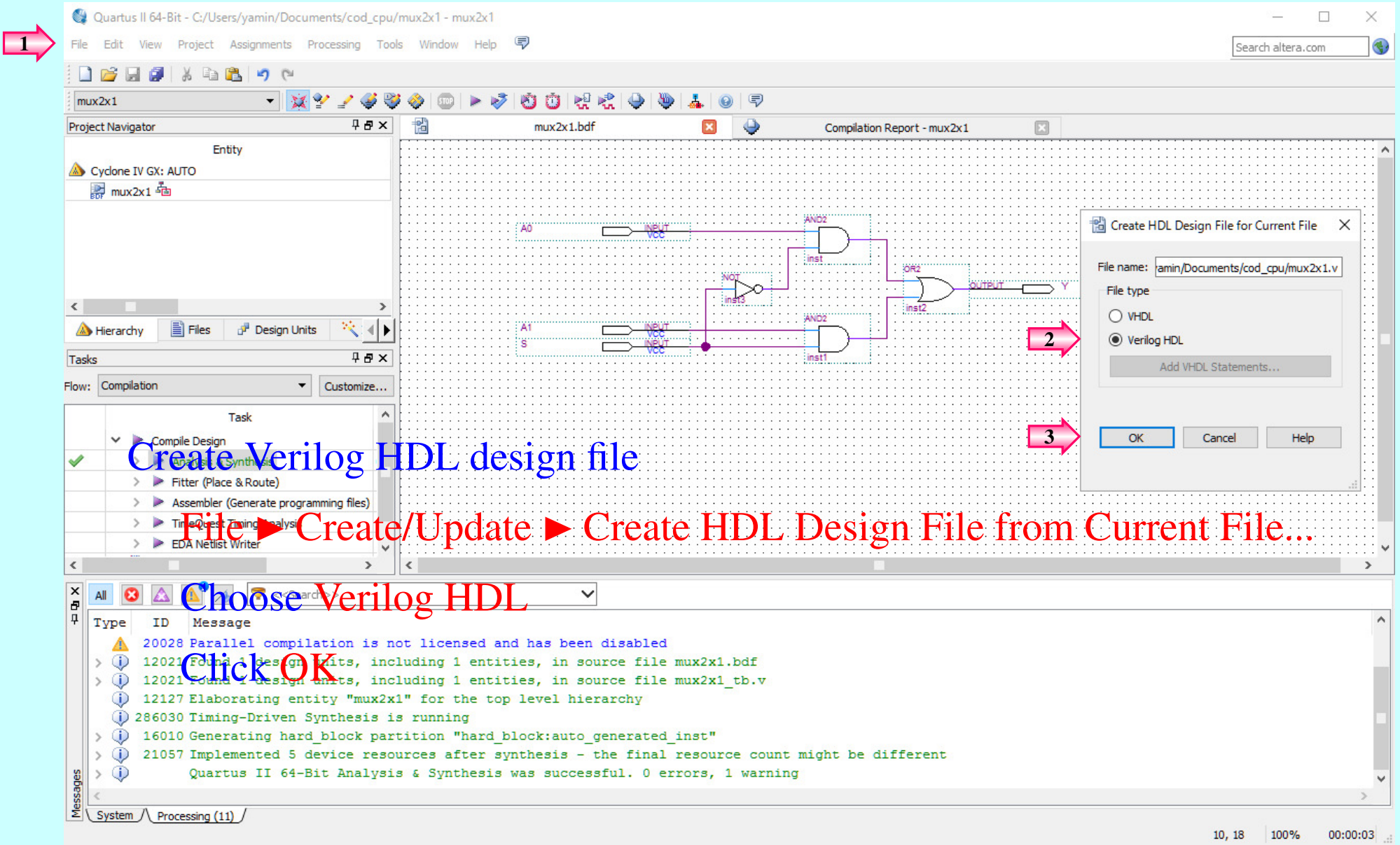
Wiring


1
Quartus II 64-Bit - C:/Users/yamin/Documents/cod_cpu/mux2x1 - mux2x1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
mux2x1
Project Navigator
Entity
Cyclone IV GX: AUTO
mux2x1
Hierarchy Files Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Block1.bdf*
A0
A1
S
INPUT
VCC
AND2
inst
NOT
inst3
OR2
inst2
OUTPUT
Y
inst1
Use mouse to connect pins with wires
File ► Save (Ctrl+s)
Click 保存 (S)
All
Type ID Message
Messages
System Processing
912, 205 0% 00:00:00

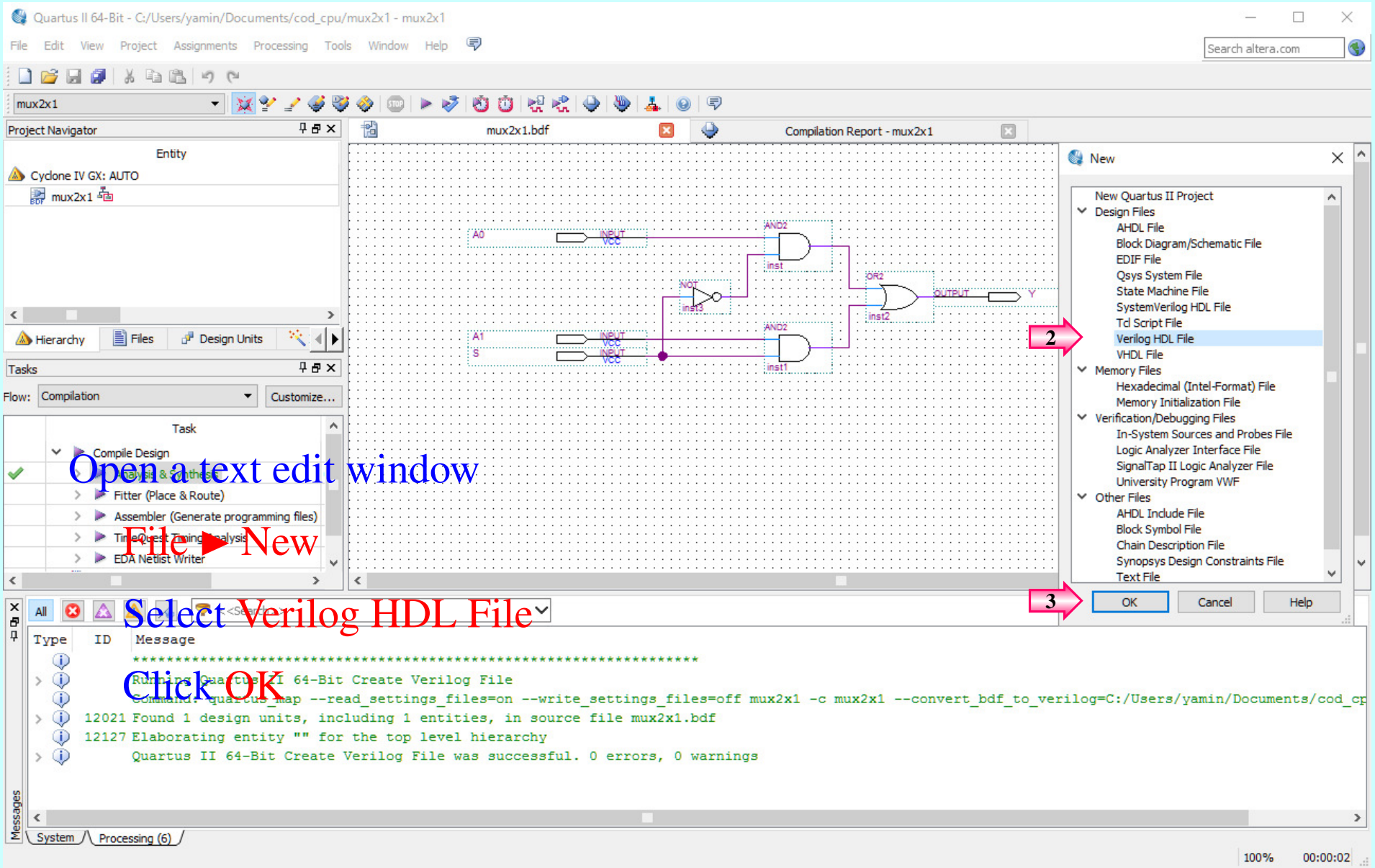
Start Analysis & Synthesis



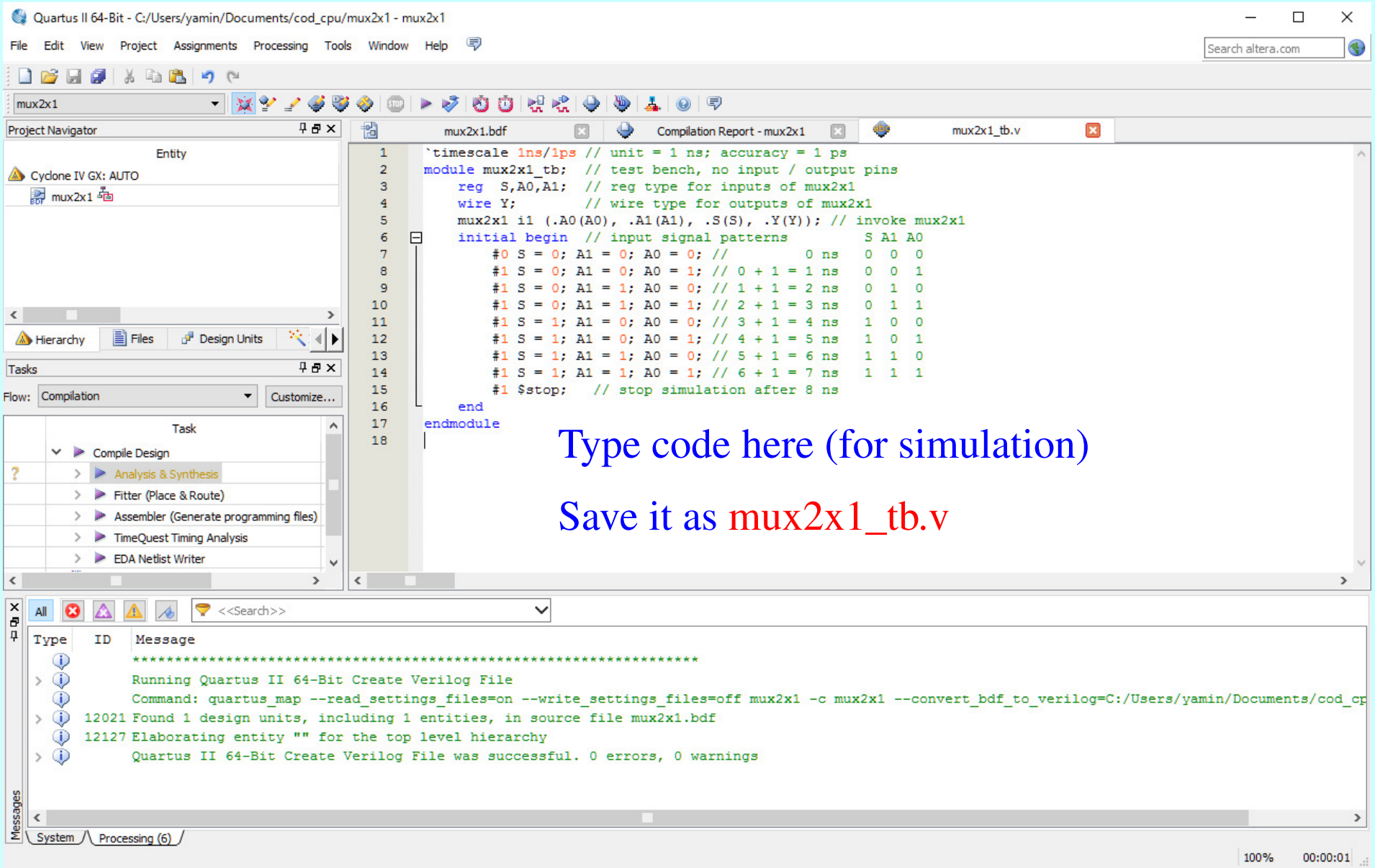
Create Verilog HDL Design File



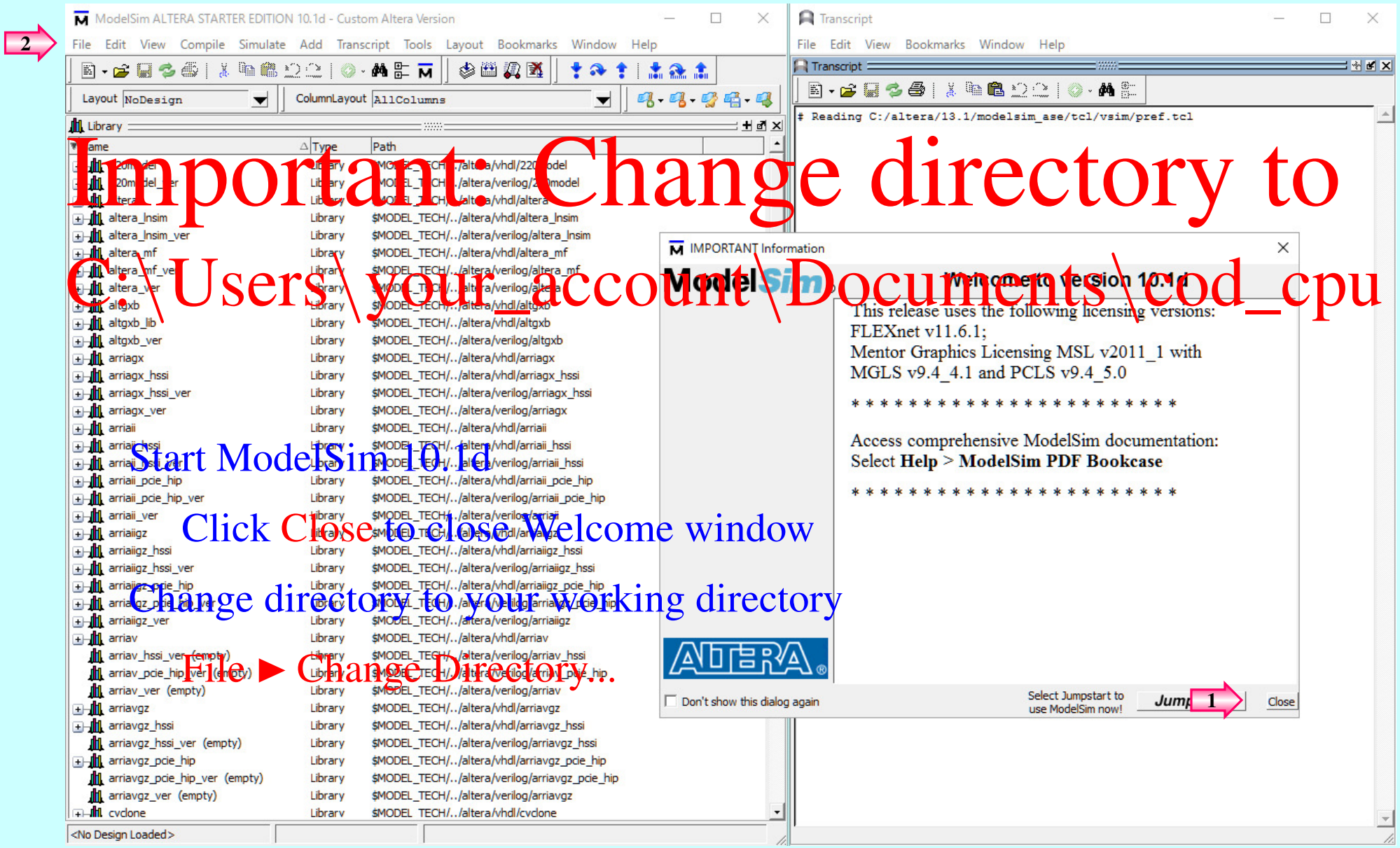
New Verilog HDL Testbench File



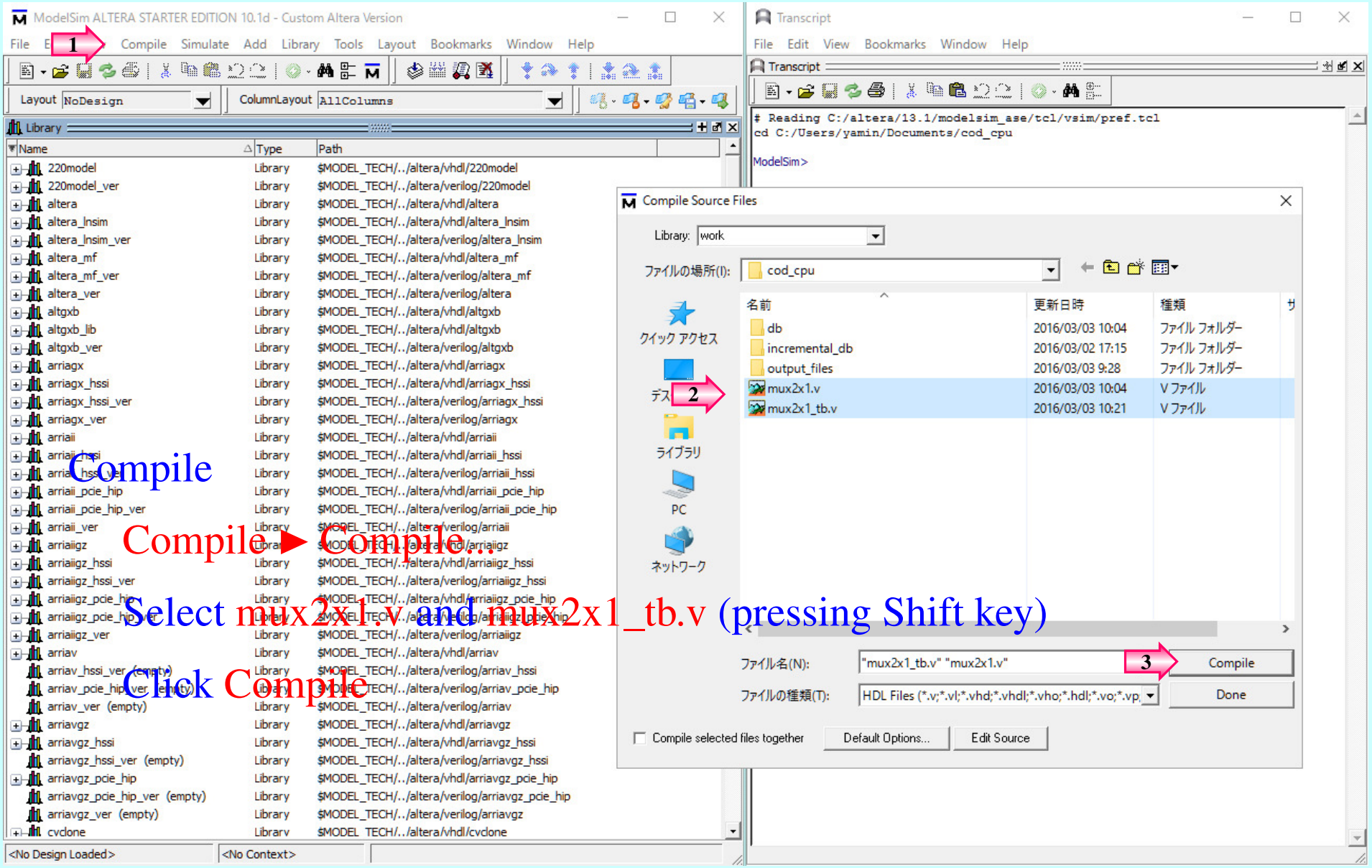
Code of Verilog HDL Testbench File



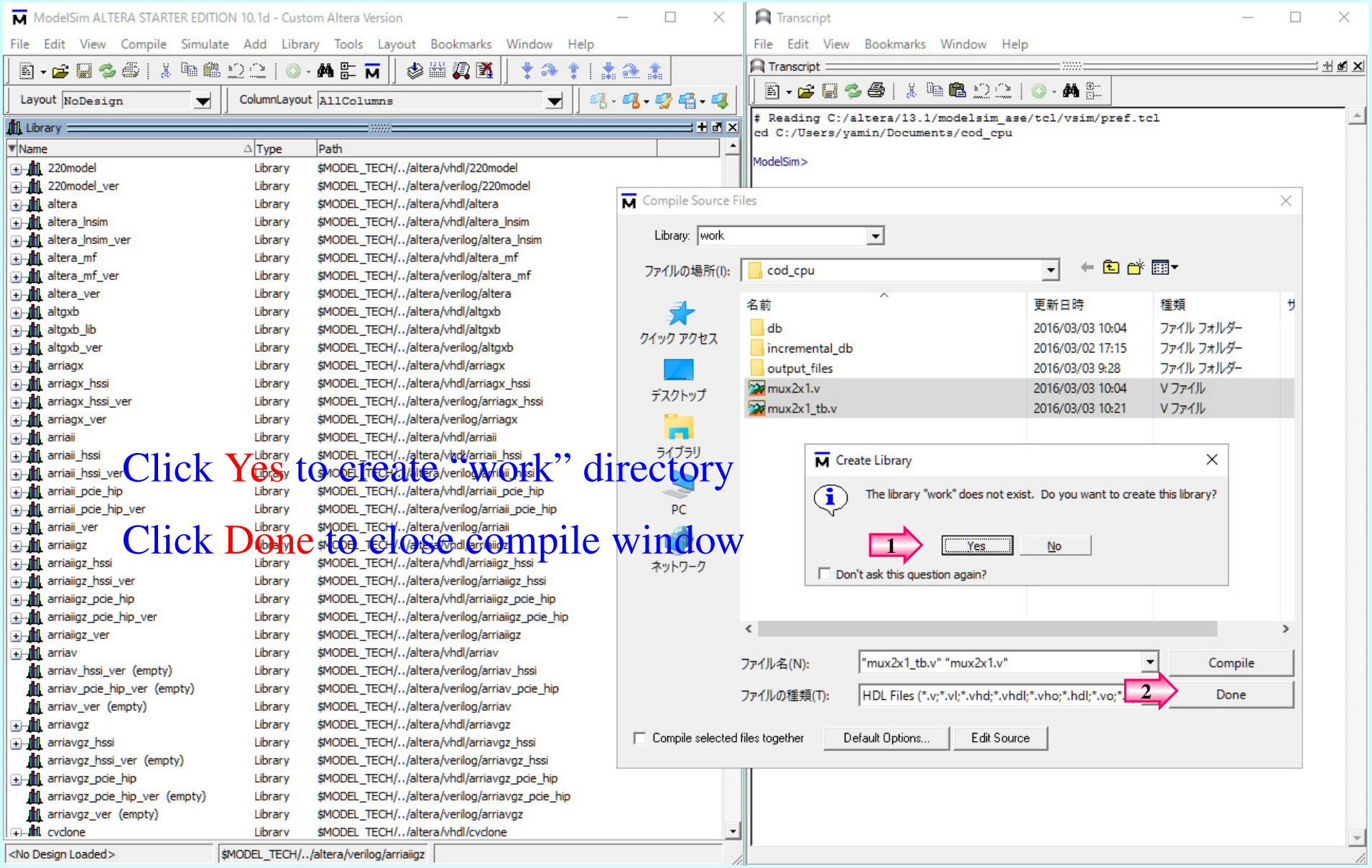
Start ModelSim-Quartus 10.1d



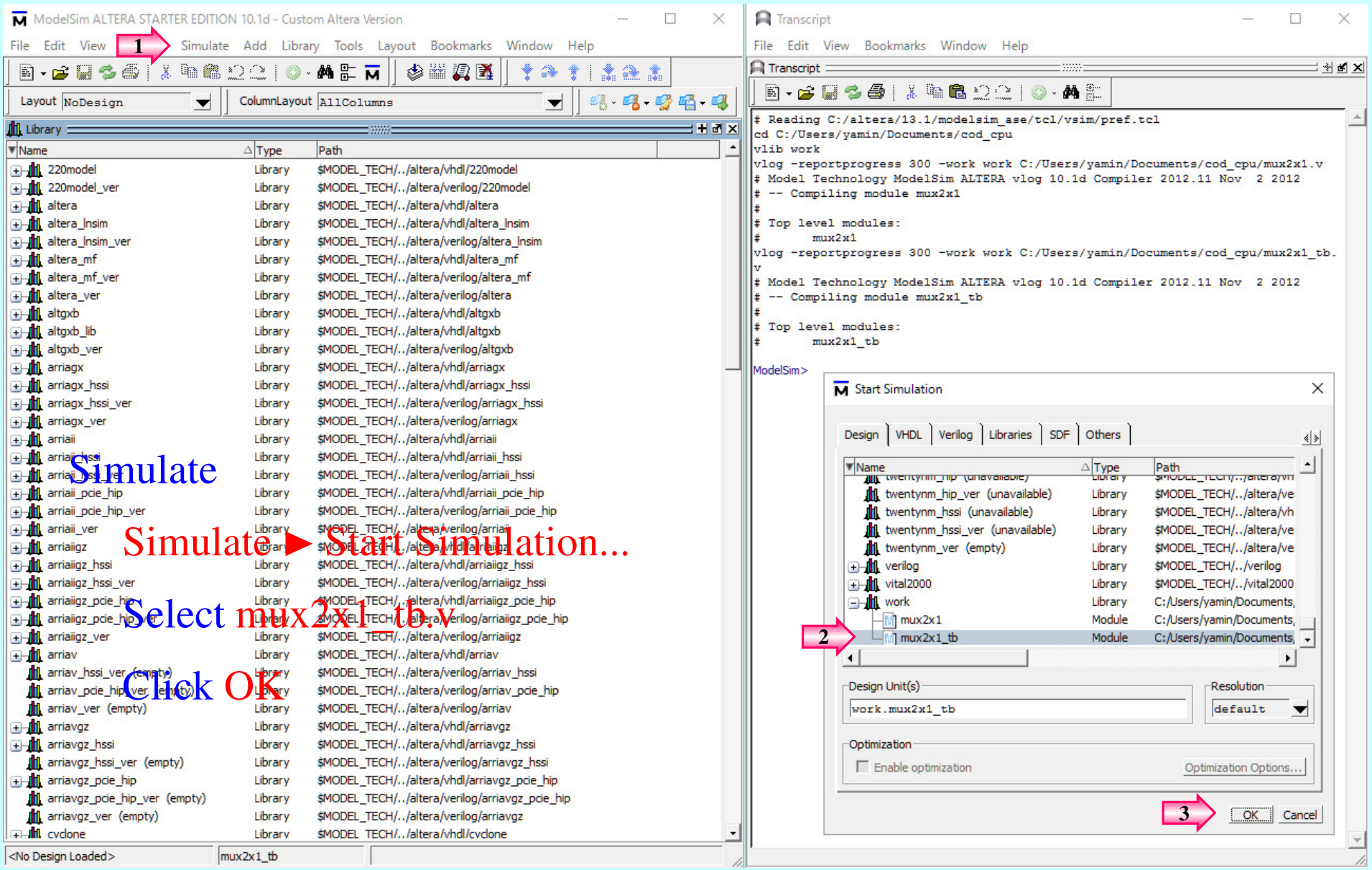
Compile mux2x1.v and mux2x1_tb.v



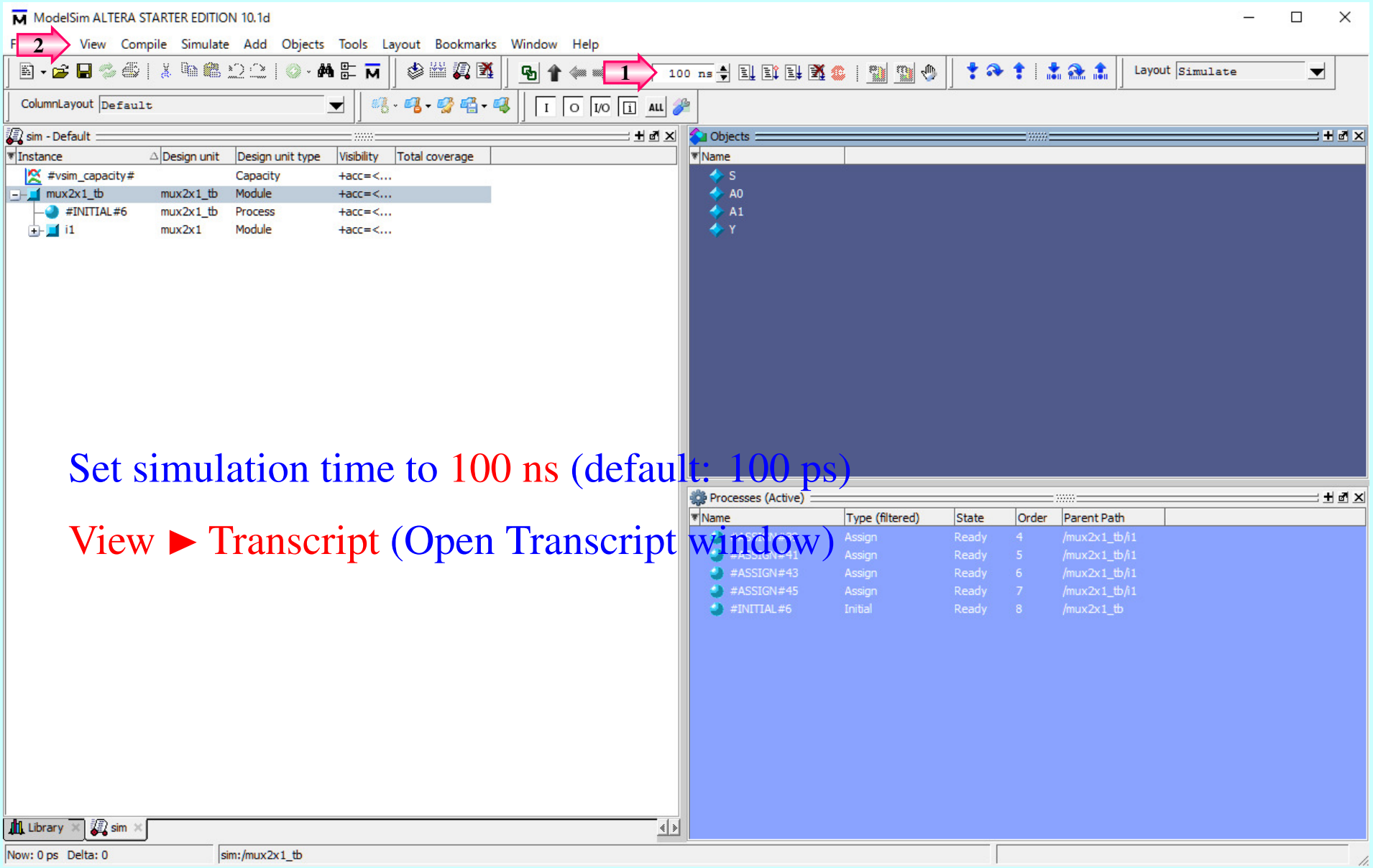
Create work Directory



Start Simulation



Change Simulation Time to 100 ns



Set simulation time to 100 ns (default: 100 ps)

View ► Transcript (Open Transcript window)

Add Signals to Wave Window

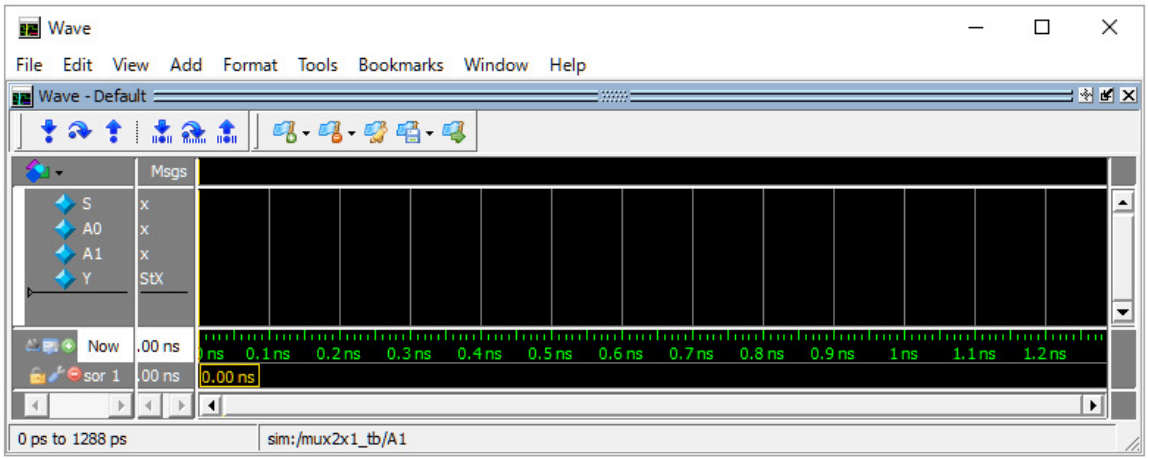
Transcript

File Edit View Bookmarks Window Help

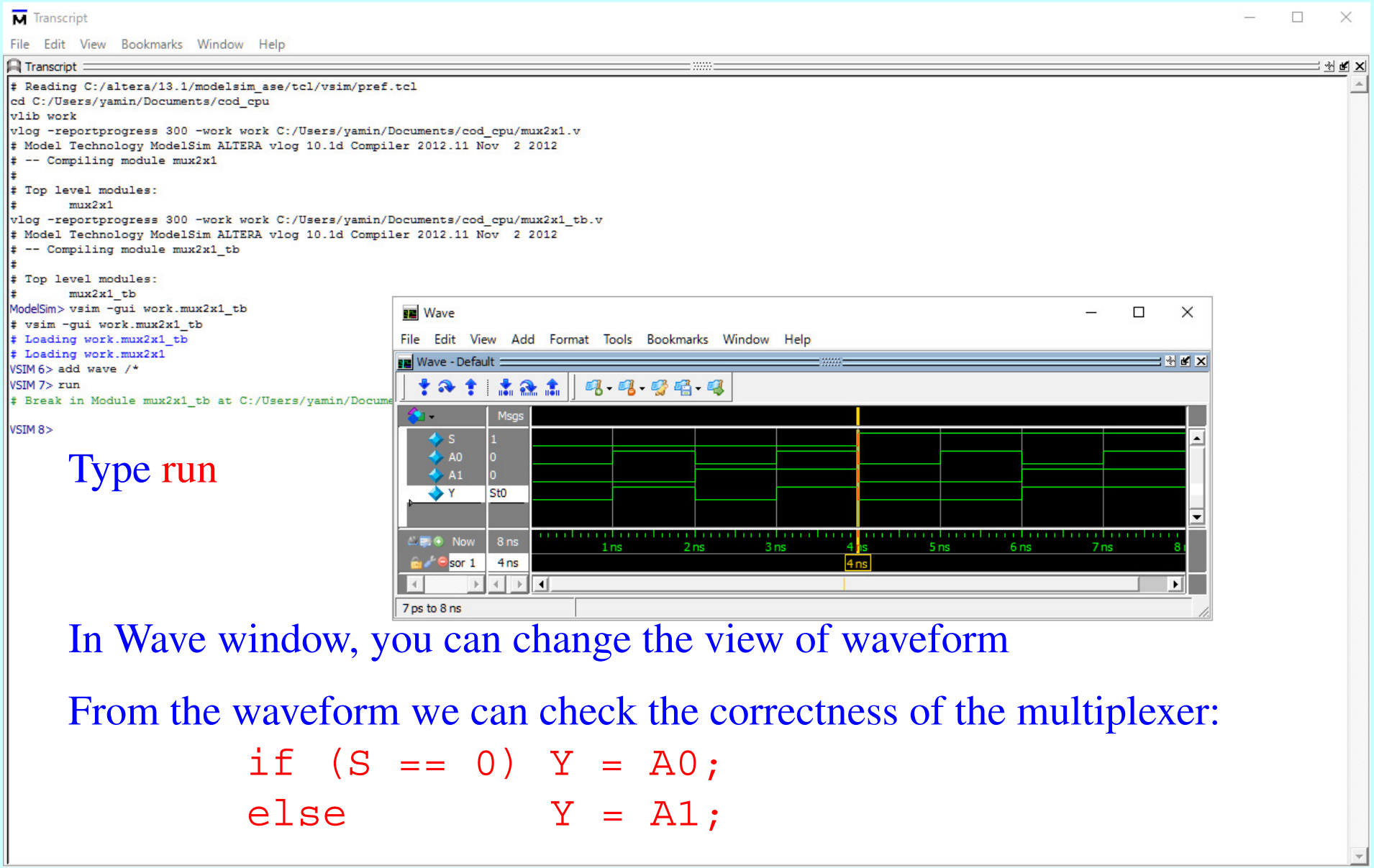
```
# Reading C:/altera/13.1/modelsim_ase/tcl/vsim/pref.tcl
cd C:/Users/yamin/Documents/cod_cpu
vlib work
vlog -reportprogress 300 -work work C:/Users/yamin/Documents/cod_cpu/mux2x1.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module mux2x1
#
# Top level modules:
#       mux2x1
vlog -reportprogress 300 -work work C:/Users/yamin/Documents/cod_cpu/mux2x1_tb.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module mux2x1_tb
#
# Top level modules:
#       mux2x1_tb
ModelSim> vsim -gui work.mux2x1_tb
# vsim -gui work.mux2x1_tb
# Loading work.mux2x1_tb
# Loading work.mux2x1
VSIM 6> add wave /*

VSIM 7>
```

1

Type add wave /*



Run Simulation



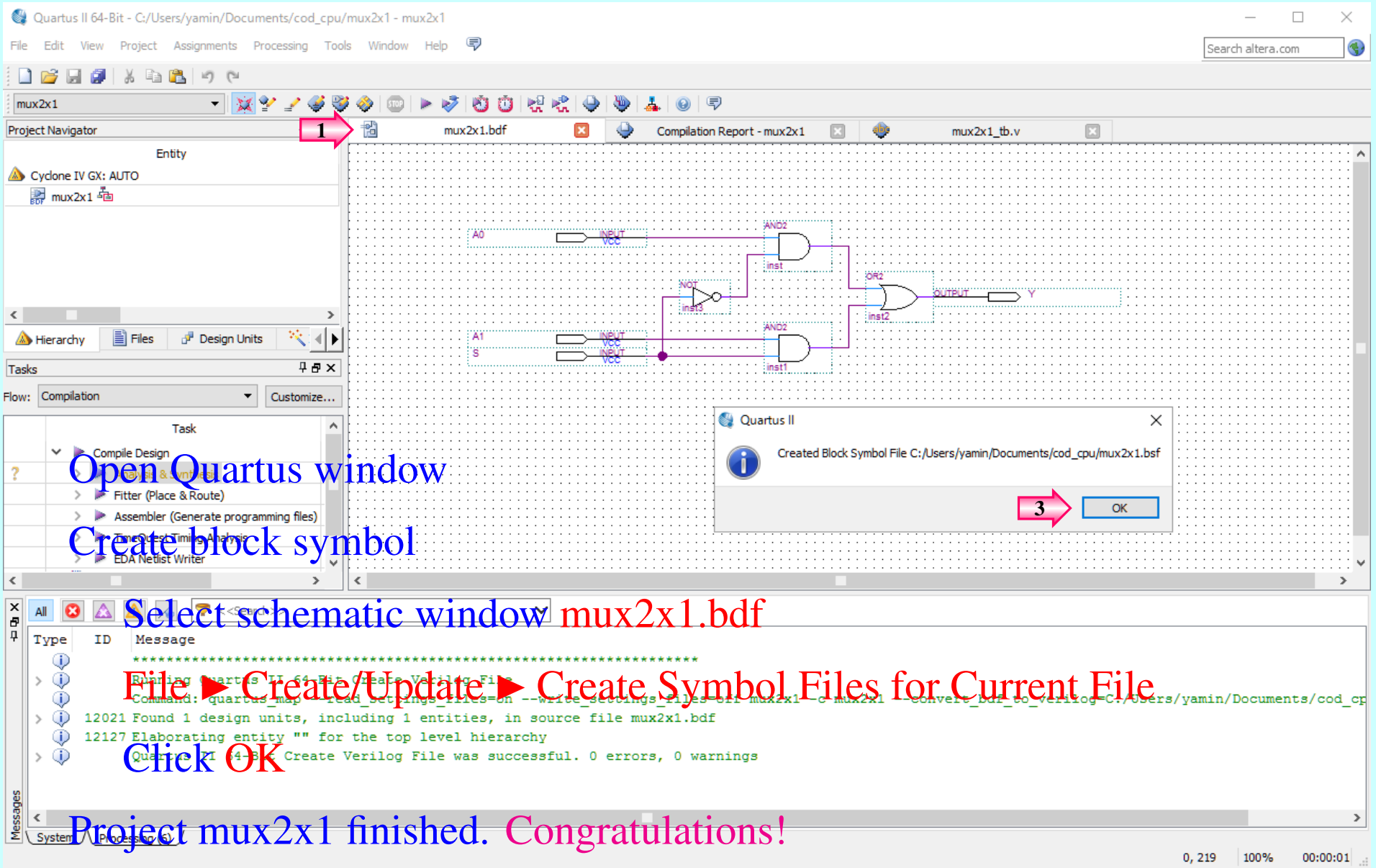
Type run

In Wave window, you can change the view of waveform

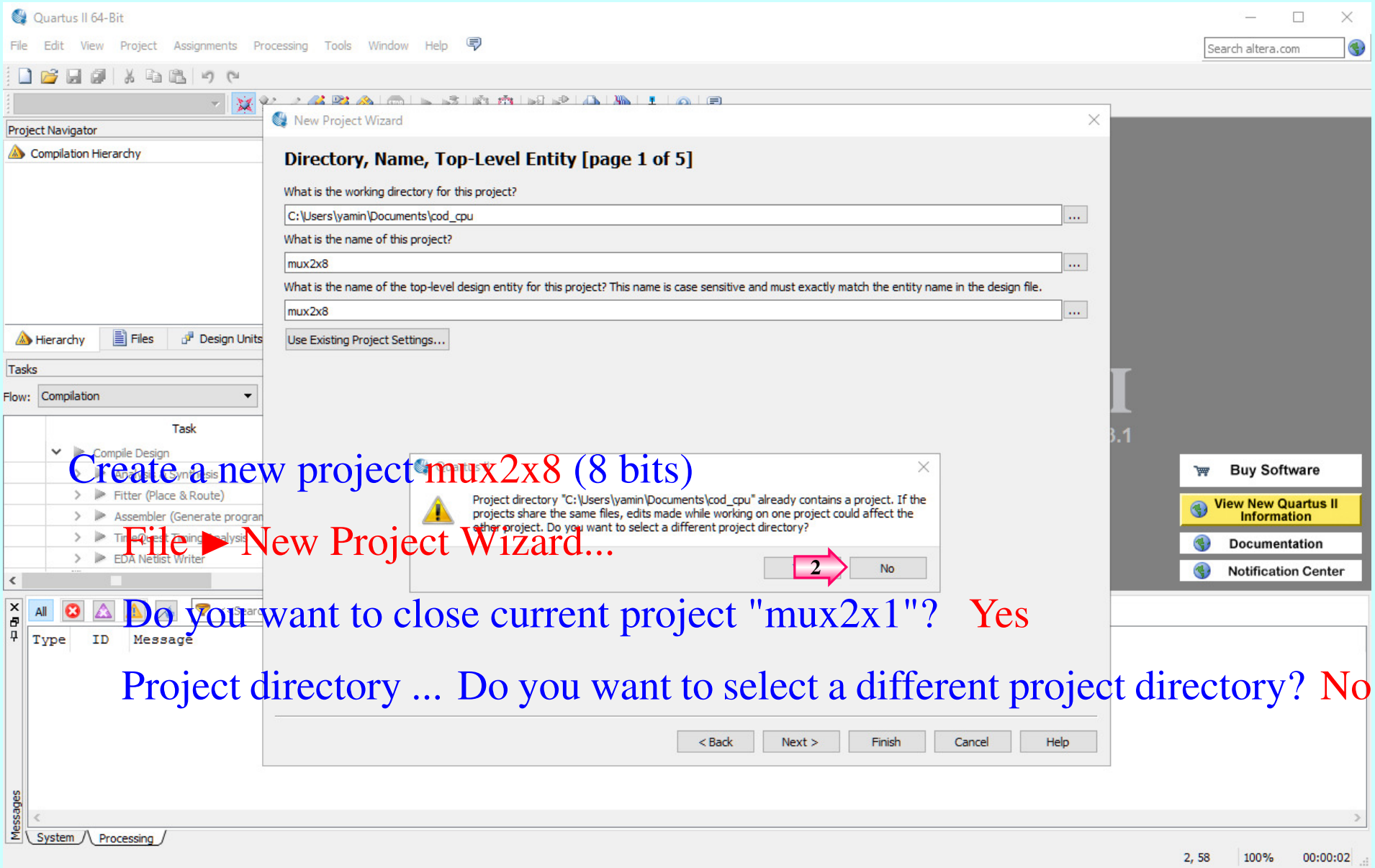
From the waveform we can check the correctness of the multiplexer:

```
if (S == 0) Y = A0;
else        Y = A1;
```

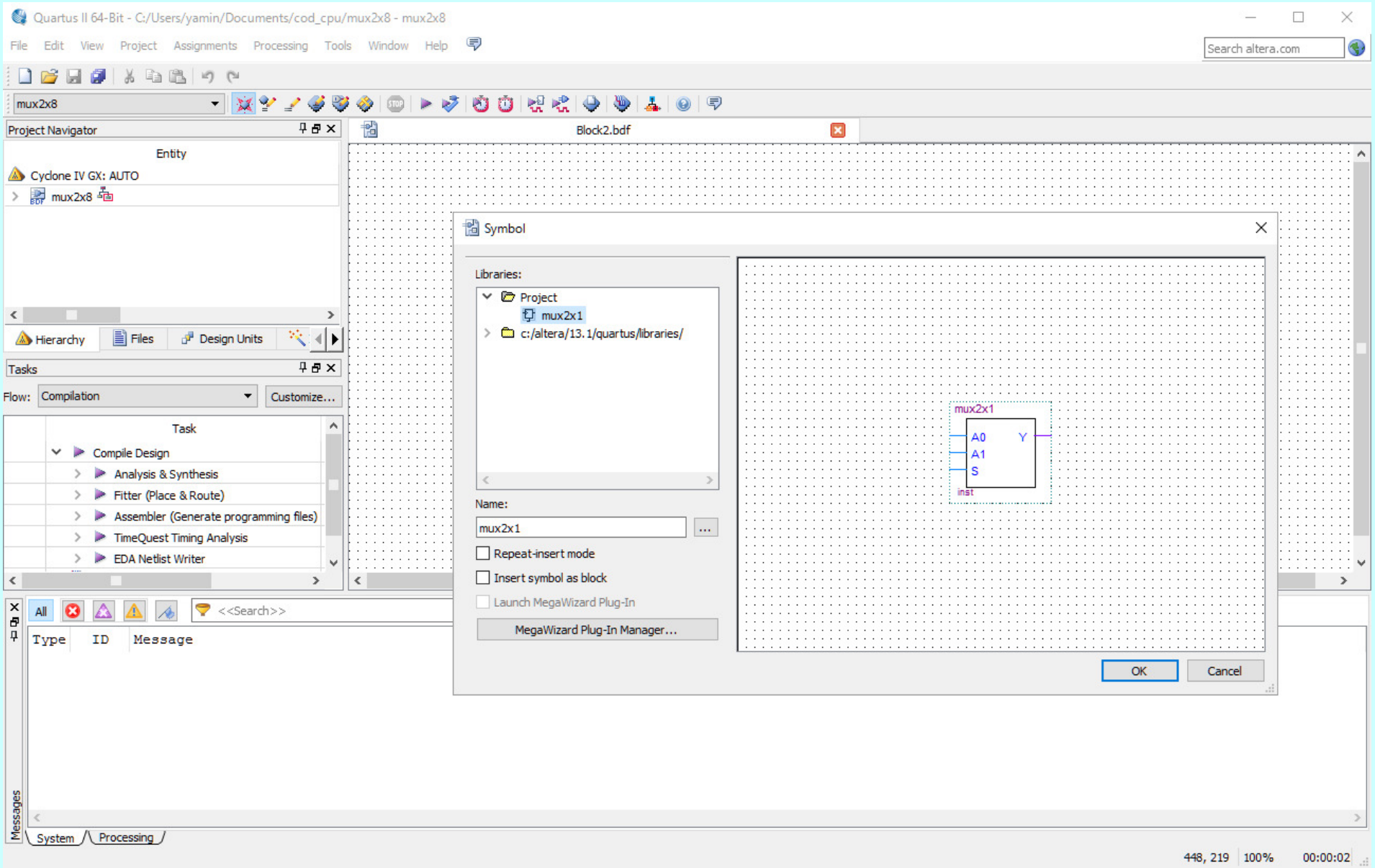
Create Block Symbol for Future Use



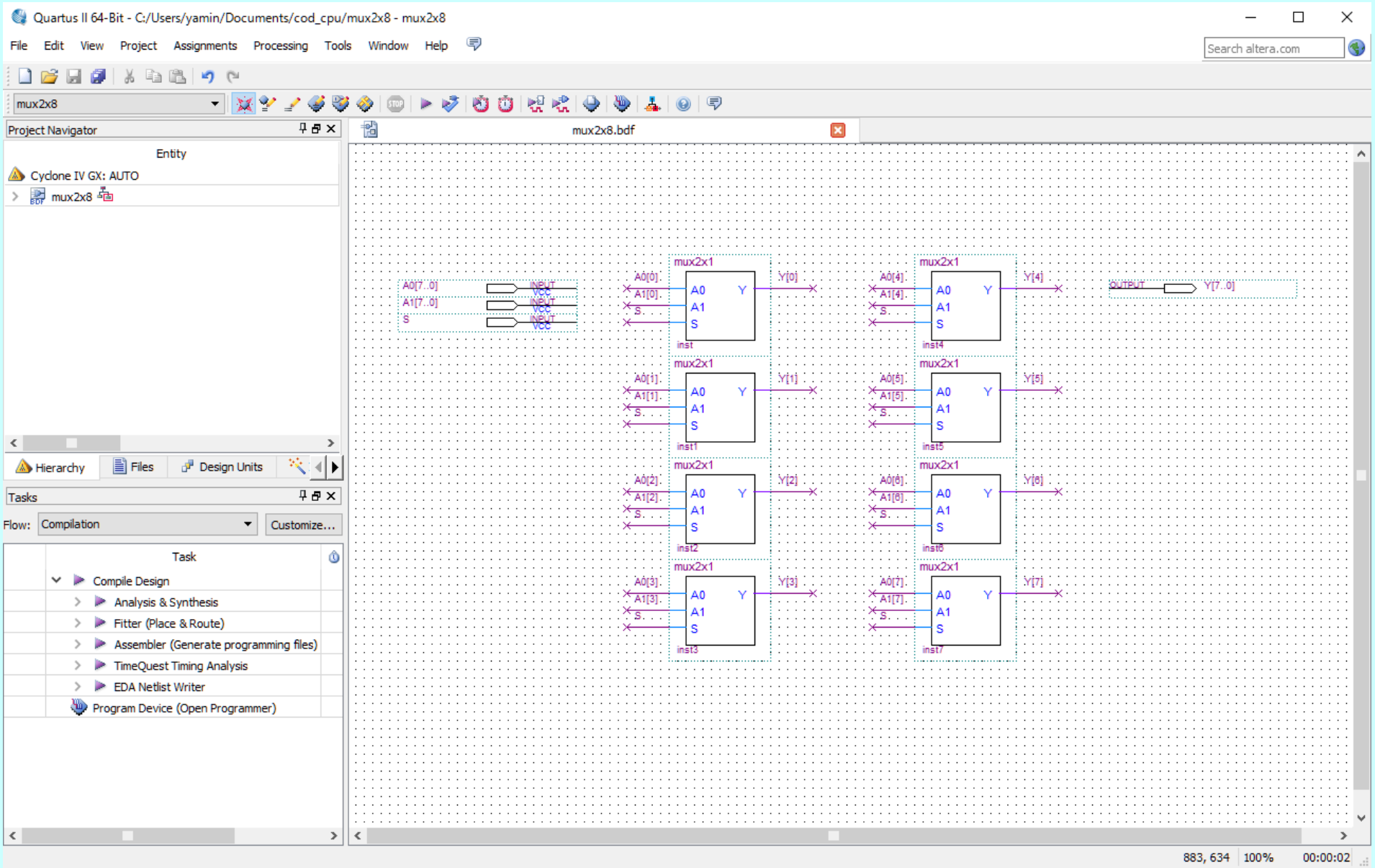
New Project — mux2x8



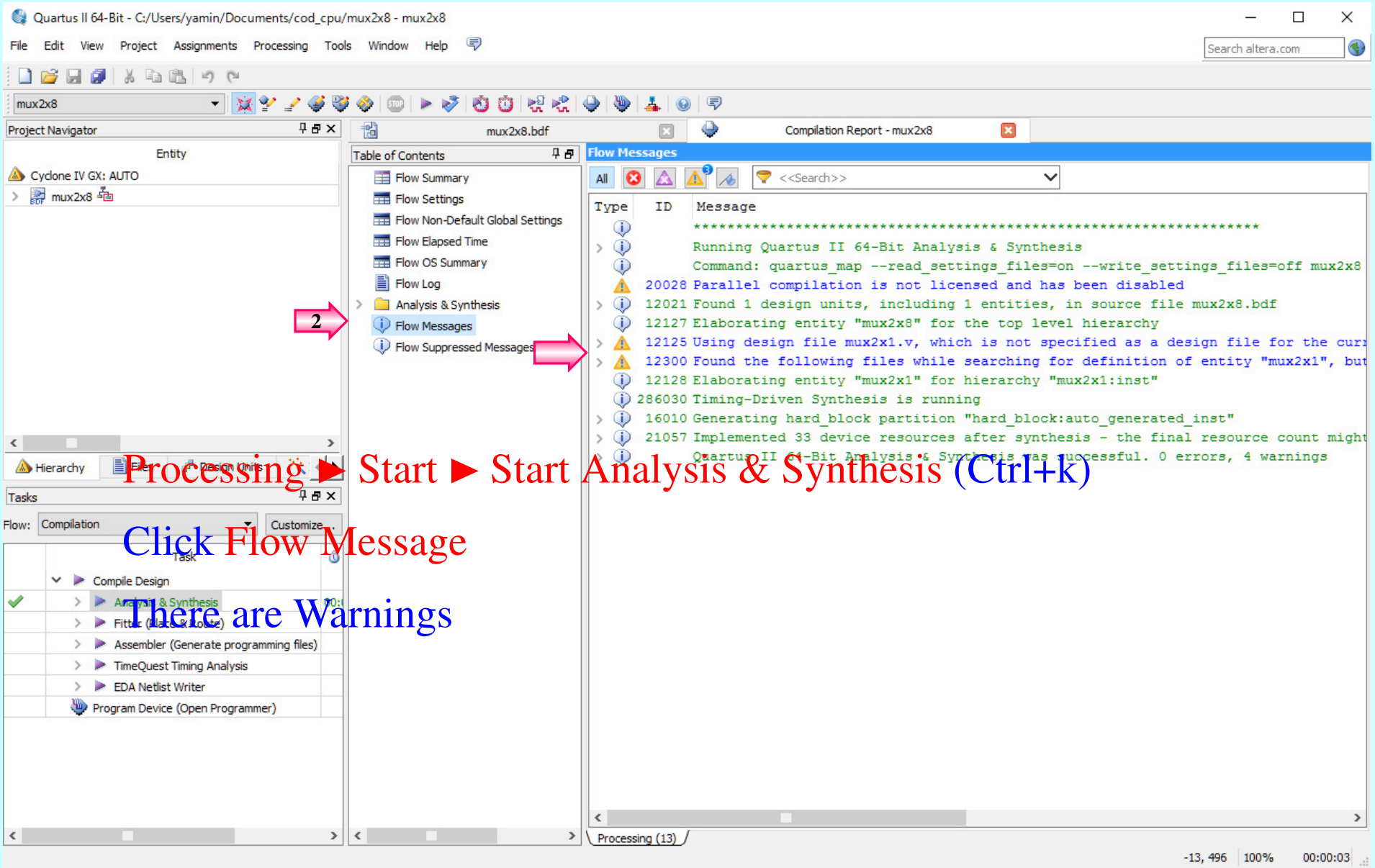
Input Components



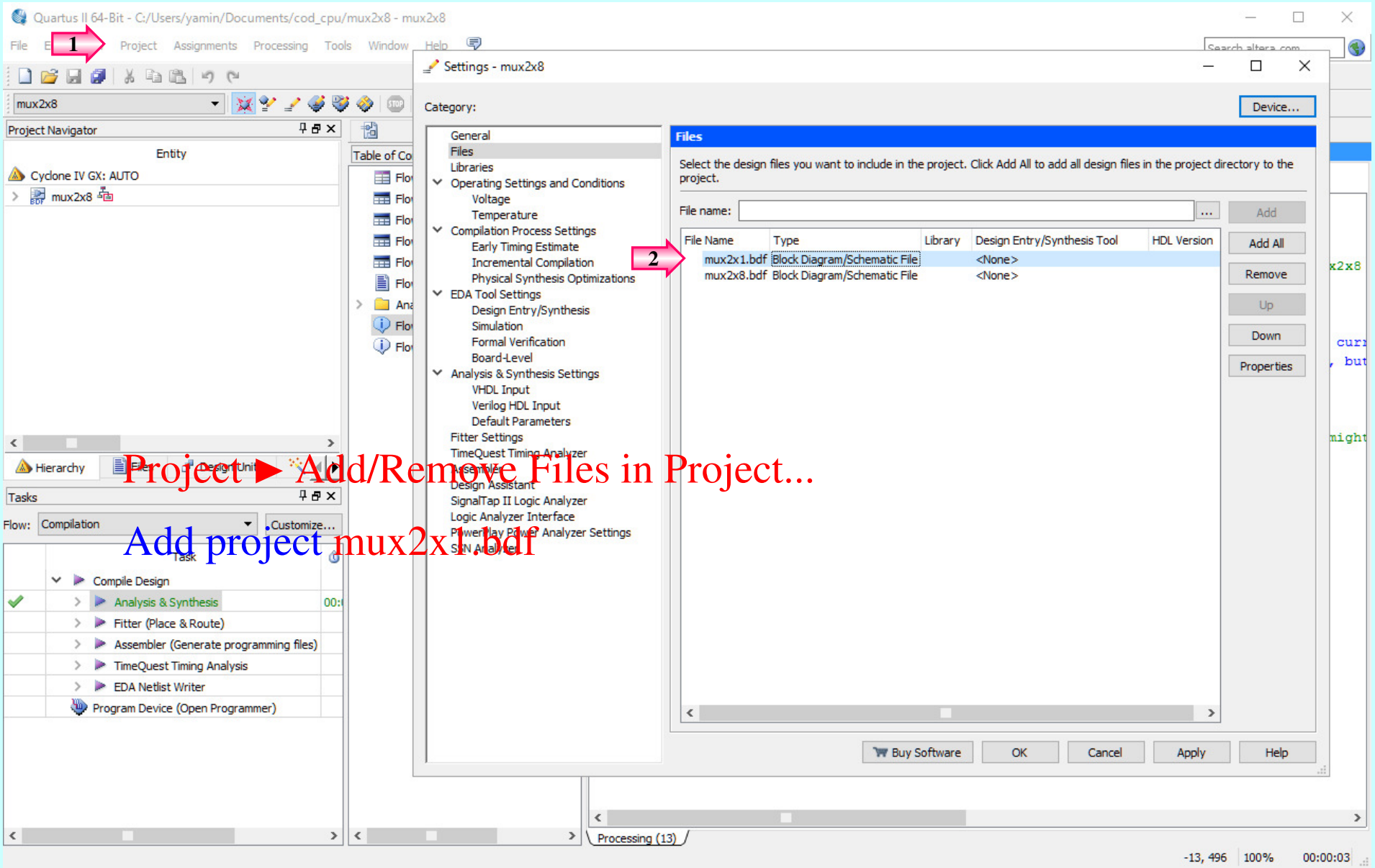
Use Wire Names to Connect Pins



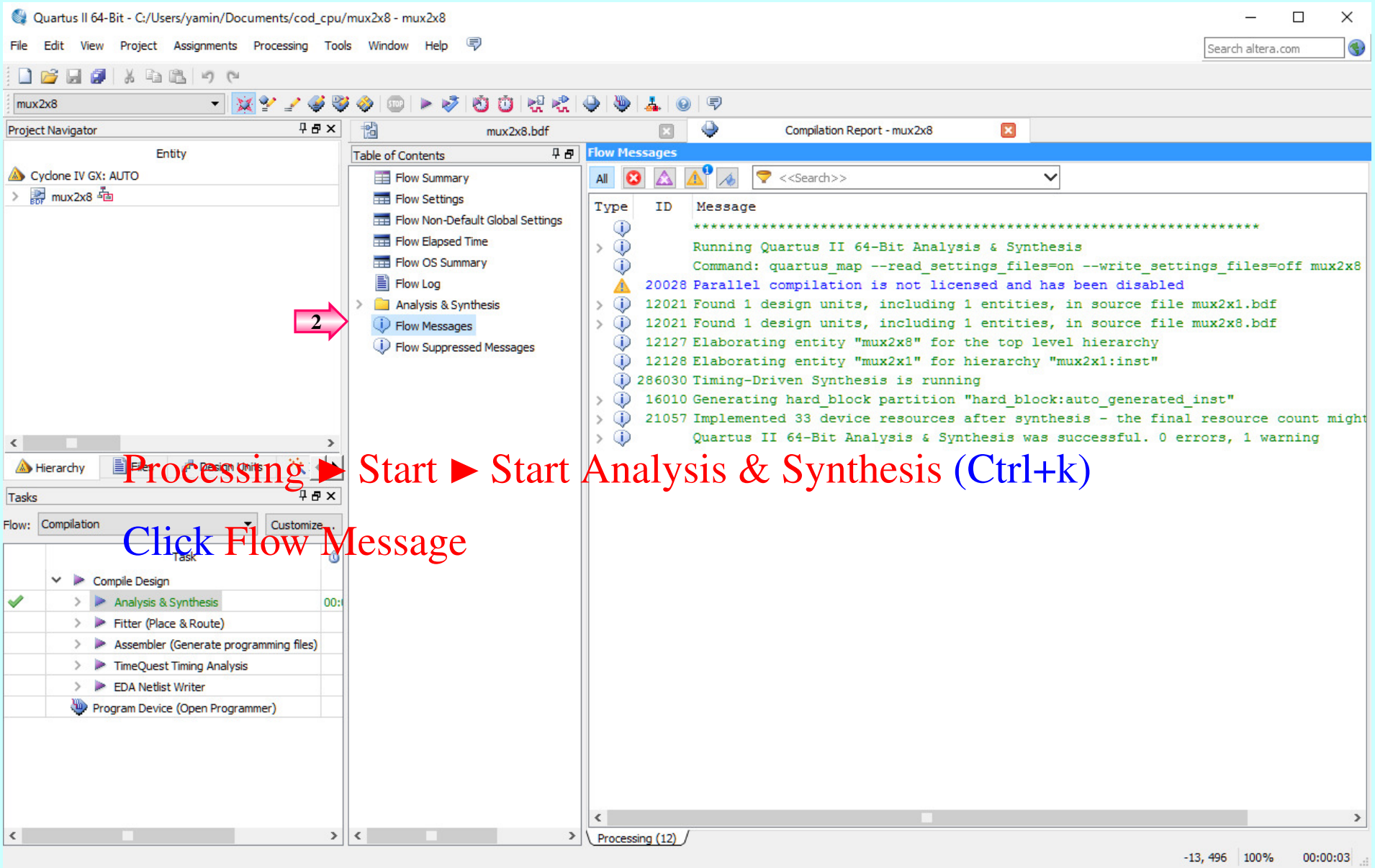
Start Analysis & Synthesis



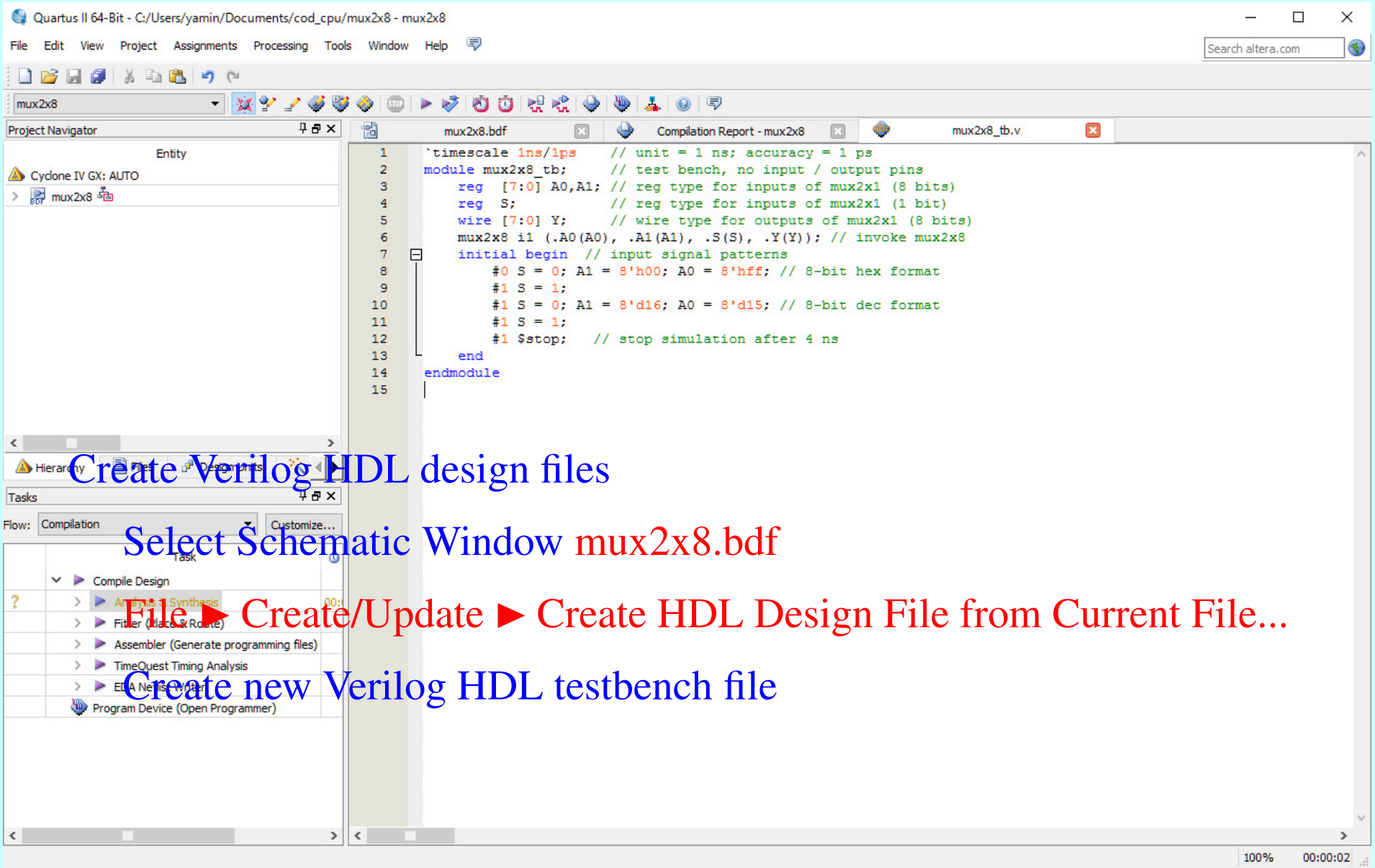
Add Project mux2x1.bdf



Start Analysis & Synthesis



Code of Testbench File mux2x8_tb.v



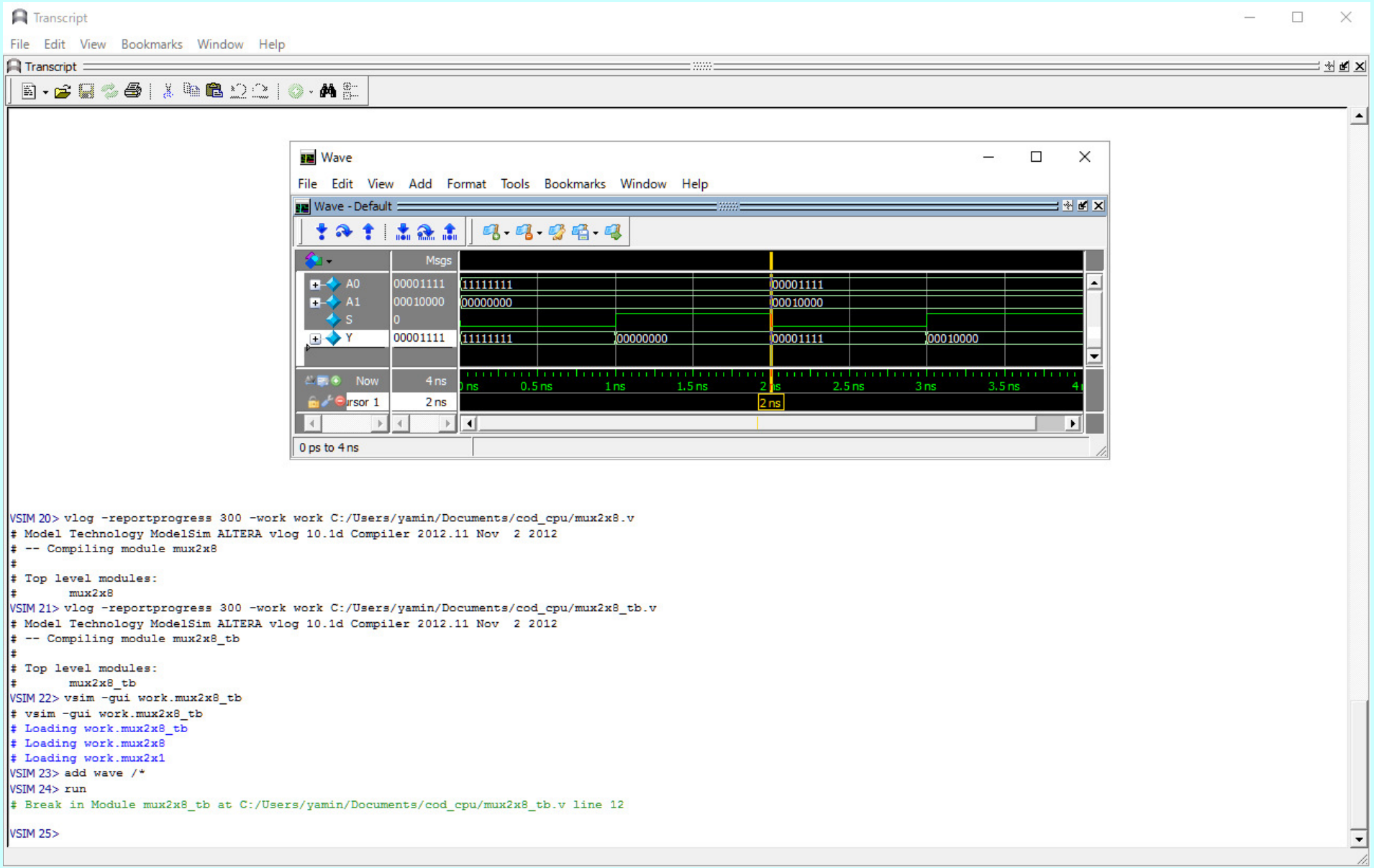
Create Verilog HDL design files

Select Schematic Window mux2x8.bdf

File ► Create/Update ► Create HDL Design File from Current File...

Create new Verilog HDL testbench file

Simulation with ModelSim



Create Block Symbol for Future Use